REMARKS

Claims 1-17 are all the claims pending in the application.

Claims 2 and 12 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly

failing to comply with the enablement requirement. With regard to the enablement rejection of

claims 2 and 12, the Examiner asserts that, as known by one of ordinary skill in the art, flash

memory must be written and erased in sections larger than the word level. The Examiner further

contends that as data in a block can only be written at once during a write operation, and the data

and meta-information are stored in a single block, there is no teaching of how the data and meta-

information can be written separately. Applicant respectfully disagrees with the Examiner's

position.

Applicant submits that the disclosure, when filed, contained sufficient information

regarding the subject matter of claims 2 and 12 as to enable one skilled in the pertinent art to

make and use the claimed invention. In particular, Applicant notes that paragraphs 66-68 of the

specification state:

> As for the data and meta-information, the data are written in the main area of the block and an LBN of meta-information is written in the spare area of the block so as to ensure the stable writing of relevant data.
>
> When the write operation for the data and LBN is completed in such a way, state information of "valid" for the flash memory 100 according to the write operation is written in the spare area of the block.
>
> If atomicity for a write operation on a block basis is ensured, the data and meta-information can be simultaneously written.

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In other words, the data and meta-information can be written simultaneously if the atomicity for a write operation on a block basis is ensured. However, as indicated by the above-cited portion of the specification, atomicity of the blocks is not required. The data and meta-information could, for example, be written at different times if the main area of the block and the spare area of the block are physically separate blocks, each capable of being written to at different times.

Therefore, Applicant respectfully submits that the disclosure, when filed, contained sufficient information regarding the subject matter of claims 2 and 15 as to enable one skilled in the pertinent art to make and use the claimed invention. Accordingly, Applicant would respectfully request that the Examiner reconsider and withdraw the enablement rejection of claims 2 and 12 under 35 U.S.C. § 112, first paragraph.

Claims 1, 3, 4, 11, 13 and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Conley (US 2002/0099904). Claims 5, 6, 8-10, 15 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Conley in view of Kim et al. (U.S. Pat. No. 6,381,176; hereinafter "Kim").

With regard to the rejection of claims 1, 3, 4, 11, 13 and 14, the Examiner asserts that if Conley is interpreted to fail to disclose anything related to state information, then "Conley must teach writ[ing] without changing the flash memory state information in a previous physical block[,]" and further, that "[i]f Conley does not disclose anything related to state information, there is no state information to change in a previous physical block, and accordingly, writes in Conley are made without changing flash memory state information written in a previous physical

block." The Examiner then concludes this point by stating that "[c]laims 1 and 11 do not recite

writing state information, they merely recite writing meta-information[.]" Applicant respectfully

disagrees with the Examiner's position.

Applicant notes that independent claim 1 recites, *inter alia*:

> the flash memory controller is configured to perform a
> write operation for writing the data and the meta-information
> allocated to the logical block in a new physical block without
> changing flash memory state information <u>written in a previous
> physical block</u> corresponding to the logical block if the previous
> write operation has been performed for the logical block.

Independent claim 11 recites a similar feature.

Thus, Applicant submits that claim 1 does not only recite writing meta-information.

Furthermore, claim 1 does not merely recite writing the data and the meta-information without

changing state information. On the contrary, claim 1 recites writing the data and the meta-

information allocated to the logical block in a new physical block without changing flash

memory state information <u>written in a previous physical block</u>.

In other words, according to the claimed invention, flash memory state information is

written in a previous physical block, and the writing of the data and the meta-information is

performed without changing what is written in the previous physical block, i.e., the flash

memory state information. Therefore, <u>the flash memory state information must have been</u>

<u>written in the previous physical block,</u> just as the language of claim 1 sets forth. Consequently,

with regard to the Examiner's first argument, Applicant again submits that Conley does not teach

or suggest anything related to state information, and that Conley cannot therefore teach or

suggest this claimed feature.

However, the Examiner further contends that the time stamp of Conley corresponds to the

claimed flash memory state information. Specifically, the Examiner states that since the time

stamp of Conley[1] can be used to distinguish between new and superceded pages,[2] the time stamp

is therefore used as the claimed "state information." Furthermore, the Examiner argues that

Conley discloses when new data is to be written to a logical block corresponding to a physical

block which is full, a new physical block is selected and the new data is written to the new

physical block without changing the original data. In support of his position, the Examiner cites

FIGS. 8 and 10, and paragraphs [0047]-[0049] of Conley. Based on our current understanding,

the Examiner's position does not appear to be entirely unreasonable.

Conley does appear to use the time stamp information to determine whether data written

in a physical block has been superceded.[3] Moreover, Conley appears to use this information to

avoid overwriting valid data (i.e., not superceded) in a previously written block. As a result,

Conley does not change previously written time stamp information in a valid, previously written

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[1] See Conley, FIG. 10, item 43.

[2] See Conley, paragraph [0052].

[3] See Conley, paragraph [0050].

block, since the time stamp information appears to only be updated each time new data is written to the block, i.e., when the data is superceded.[4]

Applicant herein amends the independent claims to recite that the flash memory state information is <u>time independent</u>.

Applicant submits that Conley fails to teach or suggest flash memory state information which is time independent. Thus, Applicant submits that independent claims 1 and 11 are patentable over Conley for at least these reasons. Further, Applicant submits that dependent claims 3, 4, 13 and 14 are also patentable over Conley, at least by virtue of their respective dependency on independent claims 1 and 11.

Additionally, Applicant submits that neither Conley nor Kim, either alone or in combination teach the features missing Conley, as noted above. Furthermore, Applicant submits, that even assuming, *arguendo*, that Conley and Kim teach the claimed features as the Examiner asserts, Applicant submits that one of ordinary skill in the art at the time the invention was made would not have been motivated to modify Conley in view of Kim.

Regarding claims 5 and 15, the Examiner states:

> Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 50 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

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[4] See Conley, paragraph [0056].

> At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.
>
> ...
>
> The motivation for doing so would have been to determine which block will be erased during a recovery operation[.]

Applicant respectfully disagrees with the Examiner's position.

On the contrary, Applicant submits that, as the Examiner correctly notes, paragraph 50 of Conley shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the time stamps of the blocks. That is, in Conley, the time stamp is used to determine whether a block is marked for deletion or not, depending on whether the block's time stamp is out of date.[5] If the block is out of date, then it is flagged for deletion. Thus, the block is recovered through the time stamp checking, flagging and deletion of the block. Any extra recovery operations are unnecessary to the operation of Conley.

Consequently, Applicant submits that it would be unnecessary, and inefficient to the operation of Conley, to perform an extra block recovery operation as disclosed in Kim. Indeed, any such modification of Conley, as the Examiner contends, would impermissibly destroy the principle of operation of Conley.[6] Therefore, Applicant submits that one of ordinary skill in the art at the time the invention was made would not have been motivated to modify Conley in view of Kim, even assuming, *arguendo*, that the combination of the references disclose all of the claimed features, as the Examiner contends.
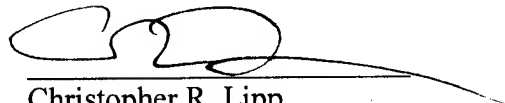
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[5] See Conley, FIG. 14 and paragraph [0052].

[6] See MPEP § 2143.02 (VI).

Accordingly, regarding the prior art rejection under 35 U.S.C. § 103, Applicant submits

that claims 5 6, 8-10, 15 and 17 are patentable over the prior art of record, for at least these

reasons.

In view of the above, reconsideration and allowance of this application are now believed

to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is

kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue

Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any

overpayments to said Deposit Account.

Respectfully submitted,

SUGHRUE MION, PLLC   Christopher R. Lipp
Telephone: (202) 293-7060   Registration No. 41,157
Facsimile: (202) 293-7860

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23373

CUSTOMER NUMBER

Date: April 10, 2007